DATA SHEET

TDA8702
8-bit video digital-to-analog converter

Product specification
Supersedes data of April 1993
File under Integrated Circuits, IC02

1996 Aug 23

Philips
Semiconductors

PHILIPS

8-bit video digital-to-analog converter TDA8702

FEATURES

- 8-bit resolution
- Conversion rate up to 30 MHz
- TTL input levels
- Internal reference voltage generator
- Two complementary analog voltage outputs
- No deglitching circuit required
- Internal input register
- Low power dissipation
- Internal 75 Ω output load (connected to the analog supply)
- Very few external components required.

APPLICATIONS

- High-speed digital-to-analog conversion
- Digital TV including:
  - field progressive scan
  - line progressive scan
- Subscriber TV decoders
- Satellite TV decoders
- Digital VCRs.

GENERAL DESCRIPTION

The TDA8702 is an 8-bit Digital-to-Analog Converter (DAC) for video and other applications. It converts the digital input signal into an analog voltage output at a maximum conversion rate of 30 MHz. No external reference voltage is required and all digital inputs are TTL compatible.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltage (peak-to-peak value)	note 2				
		Z_L = 10 kΩ	–1.45	–1.60	–1.75	V
		Z_L = 75 kΩ	–0.72	–0.80	–0.88	V
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB
f_{CLK}	maximum conversion rate		–	–	30	MHz
B	–3 dB analog bandwidth	f_{CLK} = 30 MHz; note 3	–	150	–	MHz
P_{tot}	total power dissipation		–	250	340	mW

Note

1. D0 to D7 connected to V_{CCD} and CLK connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$) are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is typically 75 Ω.
3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8702	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA8702T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

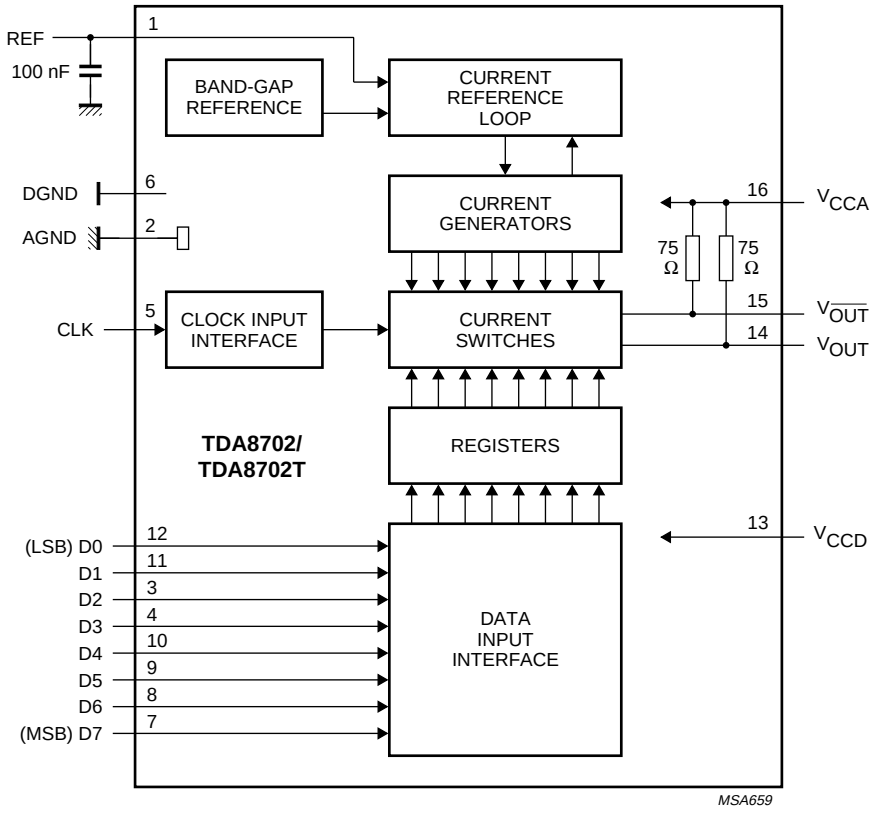


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
REF	1	voltage reference (decoupling)
AGND	2	analog ground
D2	3	data input; bit 2
D3	4	data input; bit 3
CLK	5	clock input
DGND	6	digital ground
D7	7	data input; bit 7
D6	8	data input; bit 6
D5	9	data input; bit 5
D4	10	data input; bit 4
D1	11	data input; bit 1
D0	12	data input; bit 0
V_{CCD}	13	positive supply voltage for digital circuits (+5 V)
V_{OUT}	14	analog voltage output
$V_{\overline{OUT}}$	15	complementary analog voltage output
V_{CCA}	16	positive supply voltage for analog circuits (+5 V)

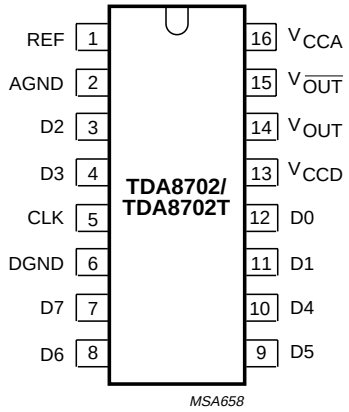


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	–0.3	+7.0	V
V_{CCD}	digital supply voltage	–0.3	+7.0	V
$V_{CCA} - V_{CCD}$	supply voltage differential	–0.5	+0.5	V
AGND – DGND	ground voltage differential	–0.1	+0.1	V
V_I	input voltage (pins 3 to 5 and 7 to 12)	–0.3	V_{CCD}	V
$I_{OUT}/I_{\overline{OUT}}$	total output current (pins 14 and 15)	–5	+26	mA
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	–	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air		
	SOT38-1	70	K/W
	SOT162-1	90	K/W

CHARACTERISTICS

$V_{CCA} = V_{16} - V_2 = 4.5$ V to 5.5 V; $V_{CCD} = V_{13} - V_6 = 4.5$ V to 5.5 V; $V_{CCA} - V_{CCD} = -0.5$ V to +0.5 V; V_{REF} decoupled to AGND by a 100 nF capacitor; $T_{amb} = 0$ °C to +70 °C; AGND and DGND shorted together; unless otherwise specified (typical values measured at $V_{CCA} = V_{CCD} = 5$ V and $T_{amb} = 25$ °C).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
I_{CCA}	analog supply current	note 1	–	26	32	mA
I_{CCD}	digital supply current	note 1	–	23	30	mA
AGND – DGND	ground voltage differential		–0.1	–	+0.1	V
Inputs						
DIGITAL INPUTS (D7 TO D0) AND CLOCK INPUT (CLK)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	$V_I = 0.4$ V	–	–0.3	–0.4	mA
I_{IH}	HIGH level input current	$V_I = 2.7$ V	–	0.01	20	µA
f_{CLK}	maximum clock frequency		–	–	30	MHz
Outputs (note 2**; referenced to V_{CCA})**						
$V_{OUT} - V_{\overline{OUT}}$	full-scale analog output voltages (peak-to-peak value)	$Z_L = 10$ kΩ	–1.45	–1.60	–1.75	V
		$Z_L = 75$ Ω	–0.72	–0.80	–0.88	V
V_{OS}	analog offset output voltage	code = 0	–	–3	–25	mV
V_{OUT}/TC	full-scale analog output voltage temperature coefficient		–	–	200	µV/K
V_{OS}/TC	analog offset output voltage temperature coefficient		–	–	20	µV/K
B	–3 dB analog bandwidth	note 3; $f_{CLK} = 30$ MHz	–	150	–	MHz
G_{diff}	differential gain		–	0.6	–	%
Φ_{diff}	differential phase		–	1	–	deg
Z_O	output impedance		–	75	–	Ω
Transfer function ($f_{CLK} = 30$ MHz)						
ILE	DC integral linearity error		–	–	±1/2	LSB
DLE	DC differential linearity error		–	–	±1/2	LSB

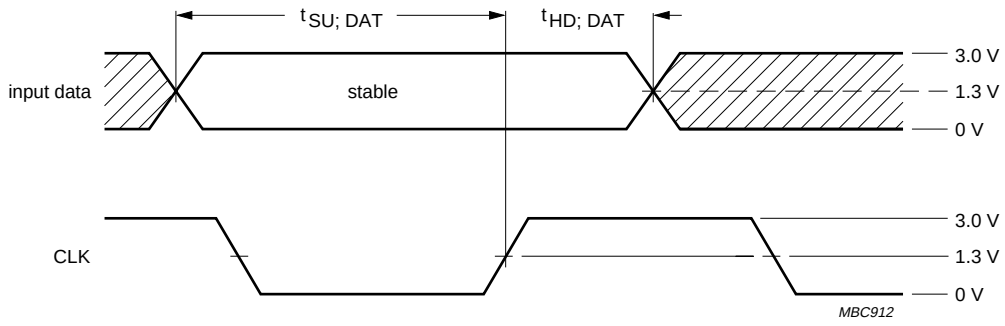
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Switching characteristics (f_{CLK} = 30 MHz); notes 4 and 5; see Figs 3, 4 and 5						
$t_{SU;DAT}$	data set-up time		–0.3	–	–	ns
$t_{HD;DAT}$	data hold time		2.0	–	–	ns
t_{PD}	propagation delay time		–	–	1.0	ns
t_{S1}	settling time	10% to 90% full-scale change to ±1 LSB	–	1.1	1.5	ns
t_{S2}	settling time	10% to 90% full-scale change to ±1 LSB	–	6.5	8.0	ns
t_d	input to 50% output delay time		–	3.0	5.0	ns
Output transients (glitches; (f_{CLK} = 30 MHz); note 6; see Fig.6						
E_g	glitch energy from code	transition 127 to 128	–	–	30	LSB.ns

Note

1. D0 to D7 are connected to V_{CCD}, CLK is connected to DGND.
2. The analog output voltages (V_{OUT} and $V_{\overline{OUT}}$ are negative with respect to V_{CCA} (see Table 1). The output resistance between V_{CCA} and each of these outputs is 75 Ω (typ.).
3. The –3 dB analog output bandwidth is determined by real time analysis of the output transient at a maximum input code transition (code 0 to 255).
4. The worst case characteristics are obtained at the transition from input code 0 to 255 and if an external load impedance greater than 75 Ω is connected between V_{OUT} or $V_{\overline{OUT}}$ and V_{CCA}. The specified values have been measured with an active probe between V_{OUT} and AGND. No further load impedance between V_{OUT} and AGND has been applied. All input data is latched at the rising edge of the clock. The output voltage remains stable (independent of input data variations) during the HIGH level of the clock (CLK = HIGH). During a LOW-to-HIGH transition of the clock (CLK = LOW), the DAC operates in the transparent mode (input data will be directly transferred to their corresponding analog output voltages (see Fig.5).
5. The data set-up ($t_{SU;DAT}$) is the minimum period preceding the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising edge of the clock and still be recognized. The data hold time ($t_{HD;DAT}$) is the minimum period following the rising edge of the clock that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising edge of the clock and still be recognized.
6. The definition of glitch energy and the measurement set-up are shown in Fig.6. The glitch energy is measured at the input transition between code 127 to 128 and on the falling edge of the clock.

Table 1 Input coding and output voltages (typical values; referenced to V_{CCA}, regardless of the offset voltage)

CODE	INPUT DATA (D7 TO D0)	DAC OUTPUT VOLTAGES			
		Z_L = 10 KΩ		Z_L = 75 Ω	
		V_{OUT}	$V_{\overline{OUT}}$	V_{OUT}	$V_{\overline{OUT}}$
0	000 00 00	0	–1.6	0	–0.8
1	000 000 01	–0.006	–1.594	–0.003	–0.797
.	.....				
128	100 000 00	–0.8	–0.8	–0.4	–0.4
.	.....				
254	111 111 10	–1.594	–0.006	–0.797	–0.003
255	111 111 11	–1.6	0	–0.8	0



The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns after the first rising edge of the clock ($t_{SU;DAT}$ is negative; –0.3 ns). Data must be held at least 2 ns after the rising edge ($t_{HD;DAT}$ = +2 ns).

Fig.3 Data set-up and hold times.

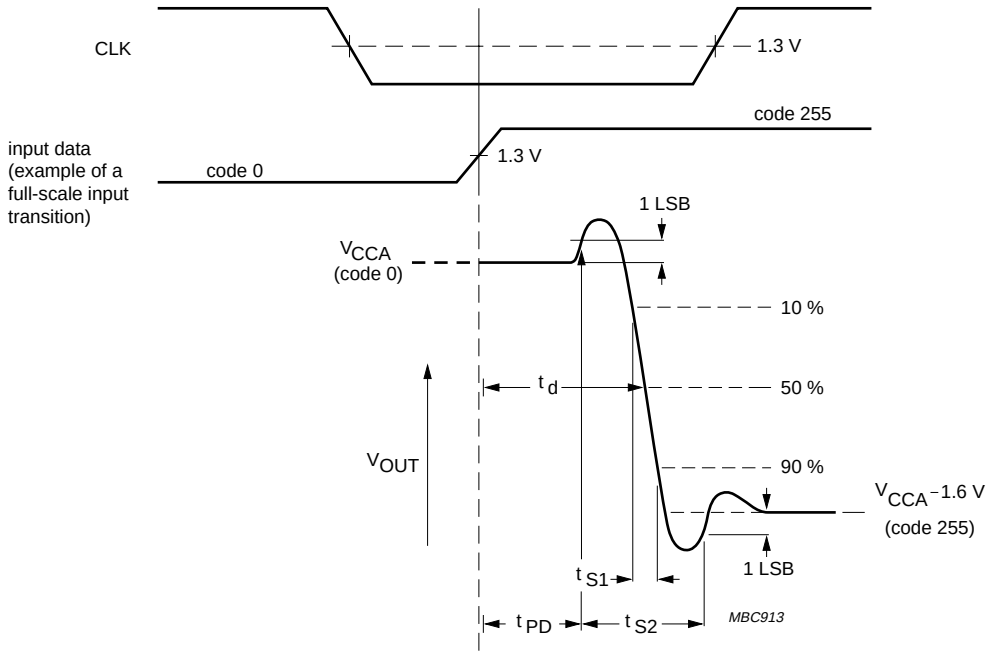
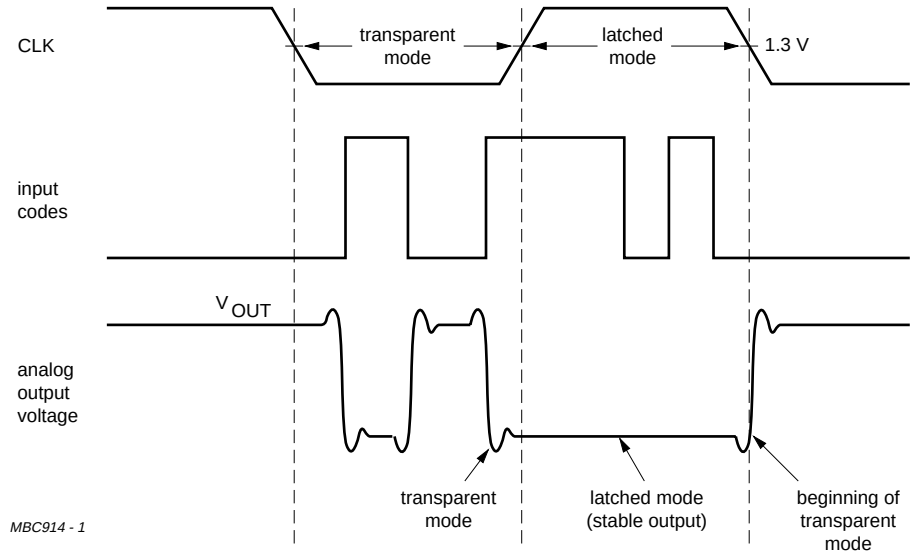
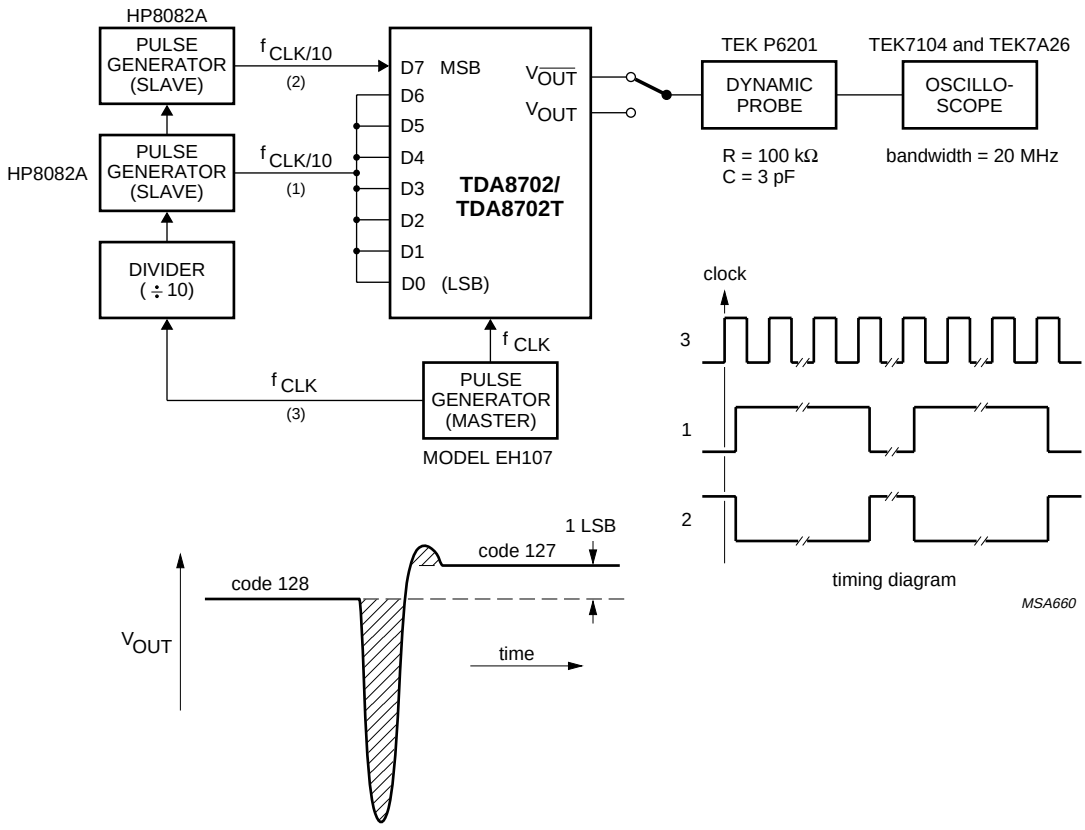


Fig.4 Switching characteristics.



During the transparent mode (CLK = LOW), any change of input data will be seen at the output. During the latched mode (CLK = HIGH), the analog output remains stable regardless of any change at the input. A change of input data during the latched mode will be seen on the falling edge of the clock (beginning of the transparent mode).

Fig.5 Latched and transparent mode.



The value of the glitch energy is the sum of the shaded area measured in LSB.ns.

Fig.6 Glitch energy measurement.

INTERNAL PIN CONFIGURATIONS

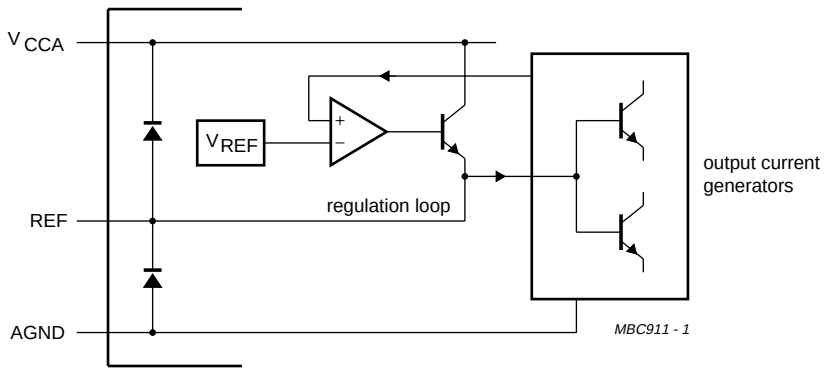


Fig.7 Reference voltage generator decoupling.

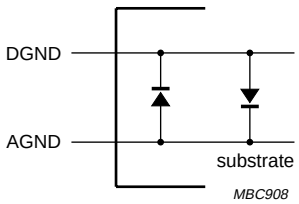


Fig.8 AGND and DGND.

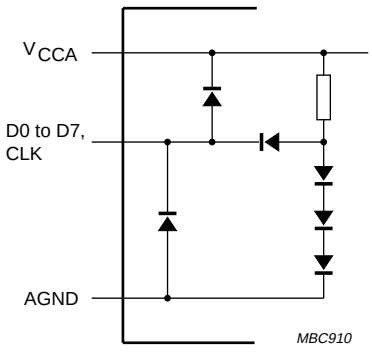


Fig.9 D7 to D0 and CLK.

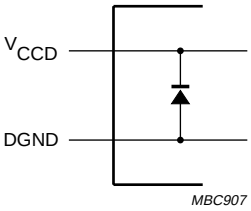


Fig.10 Digital supply.

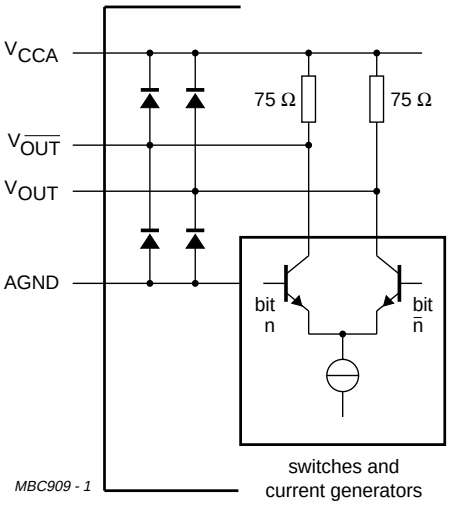


Fig.11 Analog outputs.

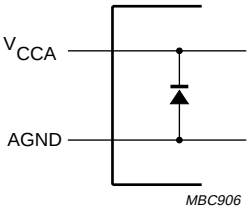
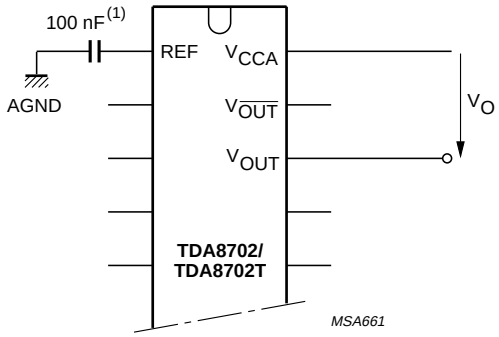


Fig.12 Analog supply.

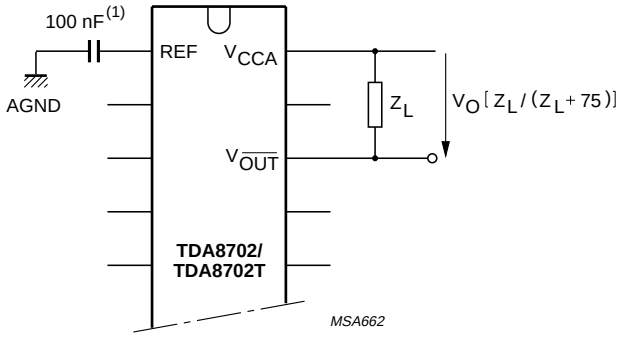
APPLICATION INFORMATION

Additional application information will be supplied upon request (please quote number FTV/8901).



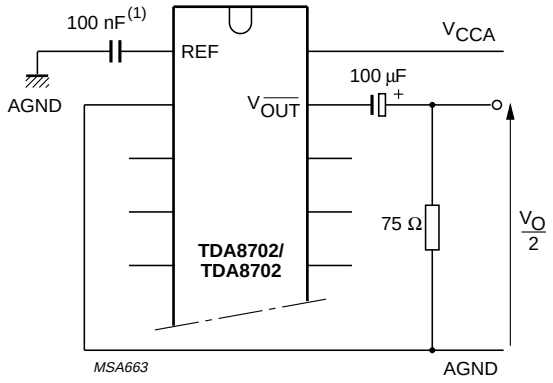
(1) This is a recommended value for decoupling pin 1.

Fig.13 Analog output voltage without external load ($V_O = -V_{\overline{OUT}}$; see Table 1, Z_L = 10 kΩ).



(1) This is a recommended value for decoupling pin 1.

Fig.14 Analog output voltage with external load (external load Z_L = 75 Ω to ∞).



(1) This is a recommended value for decoupling pin 1.

Fig.15 Analog output with AGND as reference.

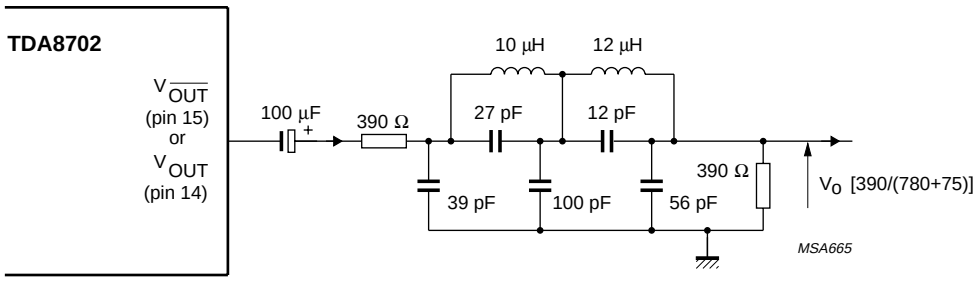
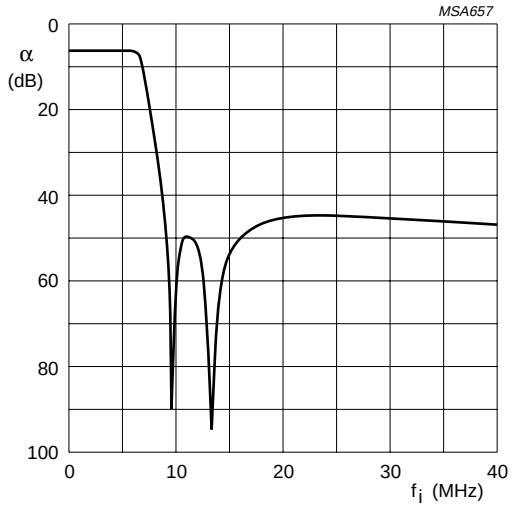
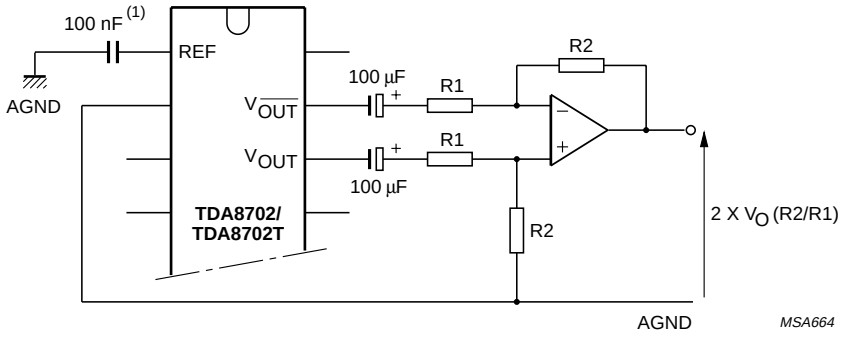


Fig.16 Example of anti-aliasing filter (analog output referenced to AGND).



Characteristics
Order 5; adapted CHEBYSHEV.
Ripple at ≤ 0.1 dB.
$f_{(-3\ dB)}$ = 6.7 MHz.
$f_{(NOTCH)}$ = 9.7 MHz and 13.3 MHz.

Fig.17 Frequency response for filter shown in Fig.16.

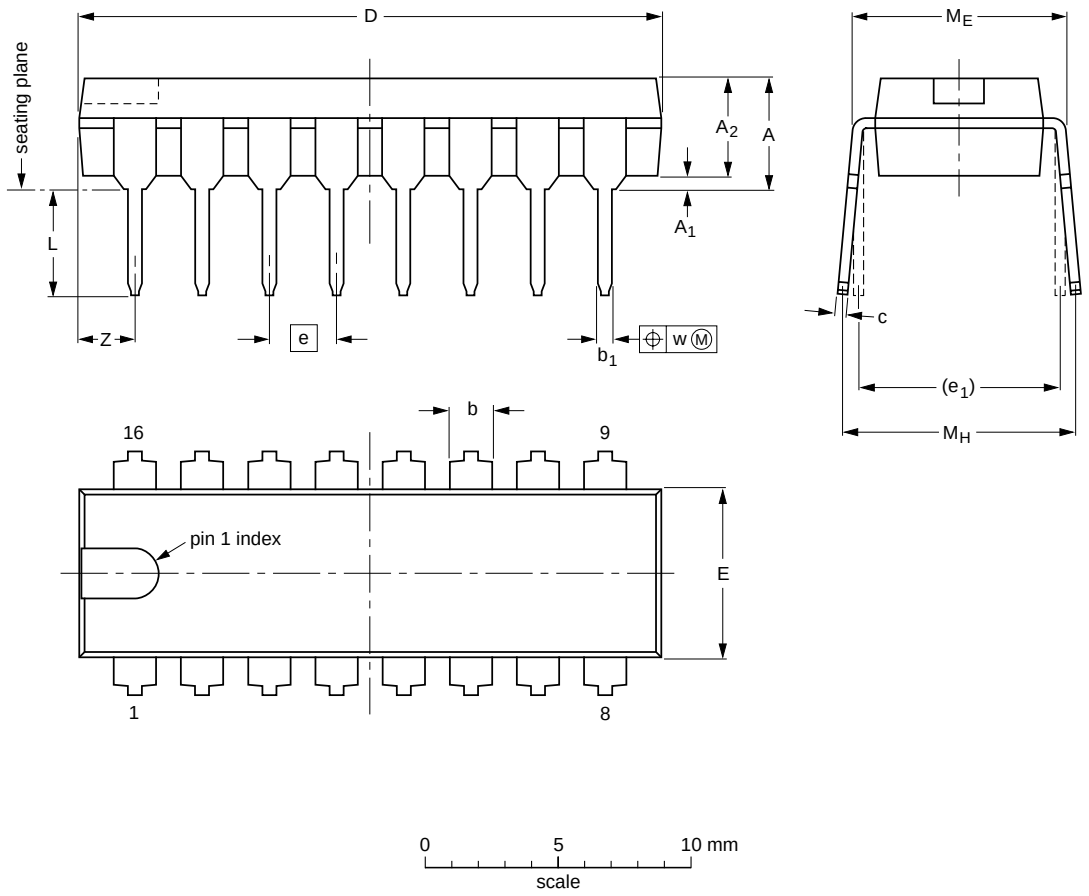


(1) This is a recommended value for decoupling pin 1.

Fig.18 Differential mode (improved supply voltage ripple rejection).

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

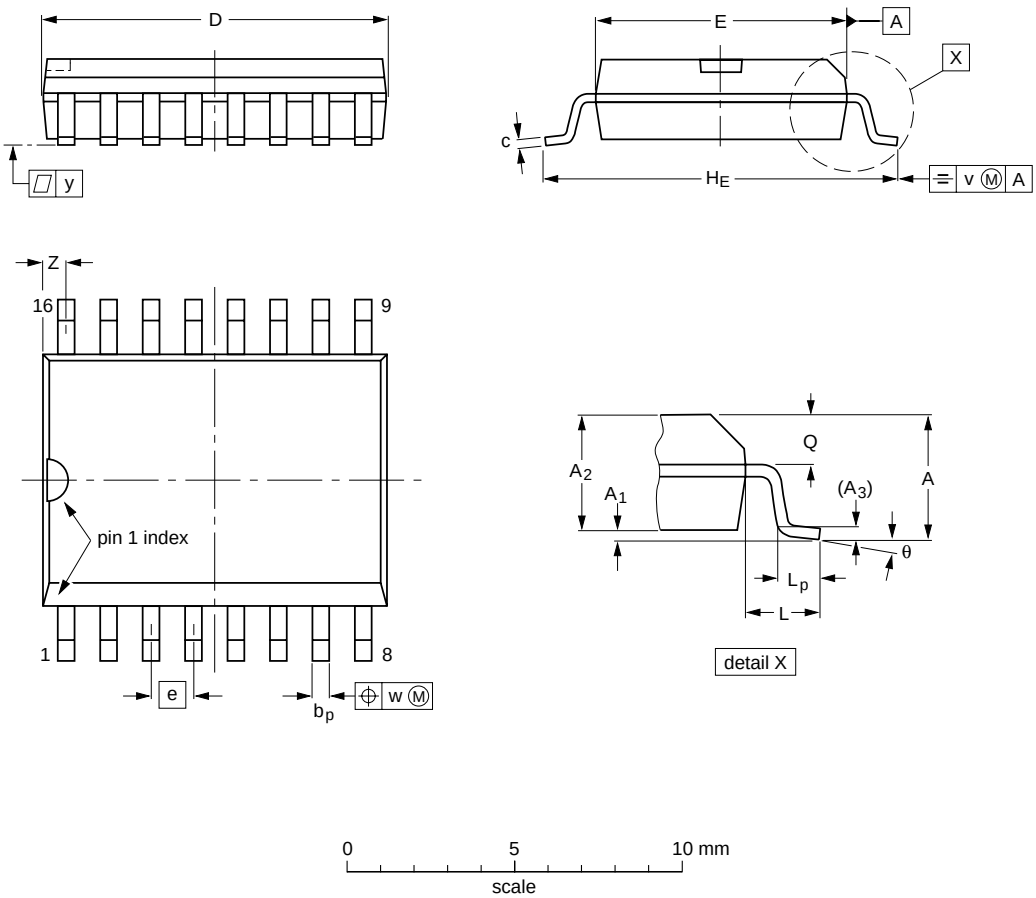
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.